A Low Distortion and High Efficiency Parallel-Operation Power Amplifier Combined in Different Phases in Wide Range of Load Impedances

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Abstract

We proposed a new four-paralleled power amplifier combined in different phases in order to accomplish a low distortion and high efficiency in wide range of load impedances. We studied them by simulation and experiment and realized an amplifier in that adjacent channel leakage power of π/4-DQPSK modulation was improved by 13dB in range of load VSWR ≤ 3 without decreasing efficiency.

1. Introduction

Recently, digital cellular phones have been popular. In their systems Japan and the United States have standardized π/4-DQPSK modulation from the viewpoint of effective frequency resources utility. As π/4-DQPSK is linear modulation, radio frequency circuits, especially power amplifiers, must avoid non-linear distortion to keep their output spectrum not expanding into adjacent channels. Several researches have been reported in order to improve linearity and efficiency of power amplifiers[1,2].

However these studies are limited only on the condition of a fixed 50Ω load, and performances under the condition of load fluctuations possibly caused by antenna condition have not been discussed. In present transmission circuits, the stabilization of load is required by inserting an isolator after a power amplifier for that reason.

In this paper we discuss a new paralleled power amplifier in order to realize low distortion and high efficiency in wide range of load impedances. It was found that distortion of a conventional amplifier was large in the limited phase area of load impedances on the smithchart. Taking a clue from these findings, we realized the low distortion and high efficiency paralleled power amplifier combined in different phases in range of load VSWR ≤ 3.

2. Characteristics of A Conventional Low Distortion Power Amplifier

So far a conventional low distortion power amplifier has been designed optimizing so that it has maximum efficiency and maximum gain property in load impedance range in which distortion performance is satisfied[3]. Figure 1(a)~(c) show measured output distortions, drain efficiencies and gains of a certain conventional amplifier at 29dBm output power with respect to the variation of load impedances. The amplifier was one stage GaAs-FET power amplifier of supply voltage 3.5V and the measured frequency was 948 MHz. A distortion property of figure 1(a) shows adjacent channel leakage power (ACP) at ±50kHz point when we use π/4-DQPSK modulation in Japan's digital cellular phone system whose specs are showed table 1. Figure 2 shows a block diagram of the measurement system. From figure 1(a)~(c), it is observed the distortion of -56.0dBc, the efficiency of 52.7% and the gain of 12.2dB with 50Ω load are the best obtained. However when the amplifier is used in range of load VSWR ≤ 3 the distortion becomes very large as -32dBc. Assume we choose the output matching network of the amplifier as satisfies the distortion in load VSWR ≤ 3, the efficiency degrades as 35%.

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In figure 1, we notice that the distortion with respect to the load impedances is especially large in the limited phase area on smithchart. Then we compare load(c) where distortion is small with load(a) where distortion is large in the fringe area of load VSWR=3 as to efficiencies and gains. It is learned that efficiency is low and gain is high for load(c), contrarily efficiency is high and gain is low for load(a). Thus, suppose two amplifiers are connected in parallel in which one has load(a) and the other has load(c), it is expected that the higher gain amplifier takes over the distortion characteristics to improve overall performance.

3. An Examination of Paralleled Power Amplifiers

For experimental study, we simulated the performances of the paralleled-amplifiers using above results. Figure 3 shows the configuration of the paralleled amplifier examined.

First we built an elemental amplifier unit and input-output characteristics of the amplifier were measured for load VSWR=3 including load(a) to load(d). Then we confirmed the distortion calculated from the measured input-output nonlinear characteristics agreed with measured values of figure 1(a). Then we estimated distortions of the paralleled amplifiers

Table 1. Specs of Japan's Digital Cellular Phone System.

item	Spec
Modulation	π/4-DQPSK
Bit Rate	42kbps
Band Width	21kHz
Adjacent Channel Leakage Power(ACP)	-45dBc (at ±50kHz)

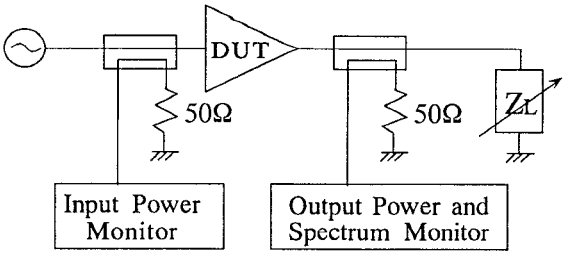

Fig. 2 Block diagram of the measurement system.

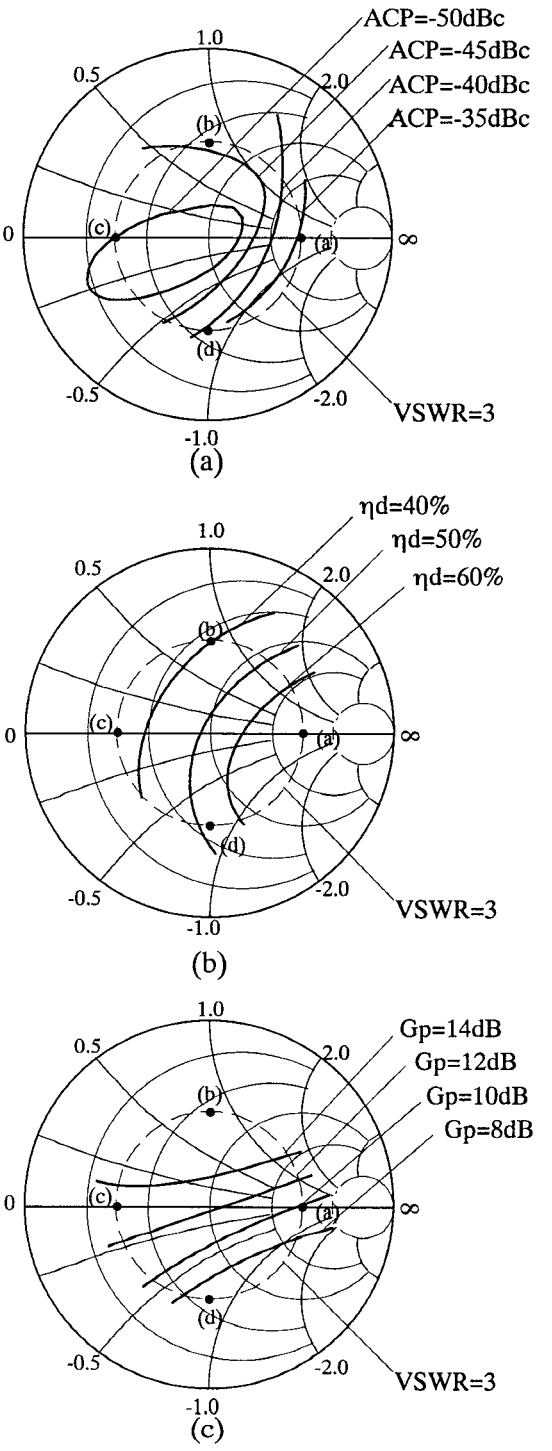

Fig. 1 Characteristics of a conventional low distortion amplifier versus load impedance at 29dBm output power.
(a) Adjacent channel leakage power (ACP)
(b) Drain efficiency
(c) Gain

shown in figure 3 for load VSWR=3 by combining each input-output characteristics measured.

Figure 3(a) shows the case of two units and the load impedance of each amplifier has 180 degree phase difference on smithchart by shifting 90 degree electrical delay. This example represents the combination of the amplifier units with load(a) and load(c) in figure 1. Output power is double of that of the elemental unit in this case.

Figure 3(b) shows the case of four units and load impedance of each unit have 90 degree electrical phase differences on smithchart. This example represents the combination of the amplifier units with load(a), load(b), load(c) and load(d) in figure 1. Output power is 4 times of that of the elemental unit in this case.

Table 2 shows the calculated results of the paralleled amplifiers of figure 3(a) and (b). Here, distortion of the paralleled amplifier is improved in comparison with the elemental amplifier. Although the two-unit amplifier did not show the sufficient performance in wide range of load impedances, the four-unit amplifier has very low distortion characteristics.

4. Experimental Results of the Four-Paralleled Power Amplifier

We built an experimental four-paralleled power amplifier based on the discussion mentioned. Figure 4 shows the configuration of the amplifier. It combines two units with Wilkinson couplers and 45 degree delay lines and four units are combined by 3dB hybrids. Figure 5 shows the performances of distortions, gains and drain efficiencies for load

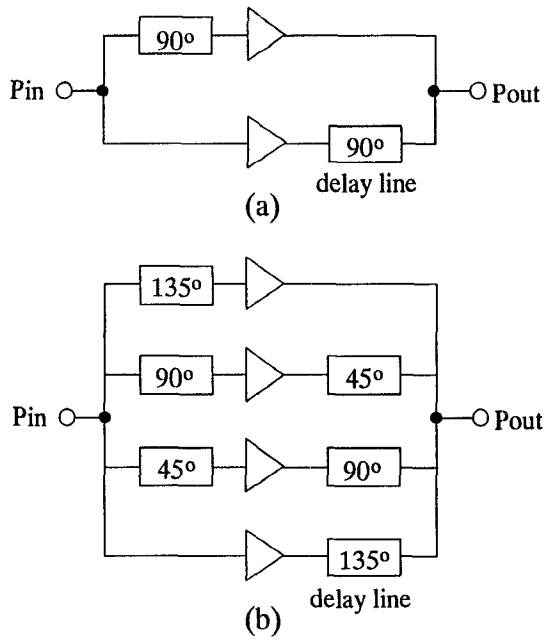

Fig. 3 Configuration of several-paralleled amplifiers.
(a) for the case of two amplifier units
(b) for the case of four amplifier units

Table 2. Results of measurement and simulation of the amplifiers for load VSWR=3.

Amplifier	ACP(dBc)	Measure./Sim.
Elemental Amp	≤ -32.0	Measurement
2 Paralleled Amp	≤ -46.5	Simulation
4 Paralleled Amp	≤ -48.8	Simulation

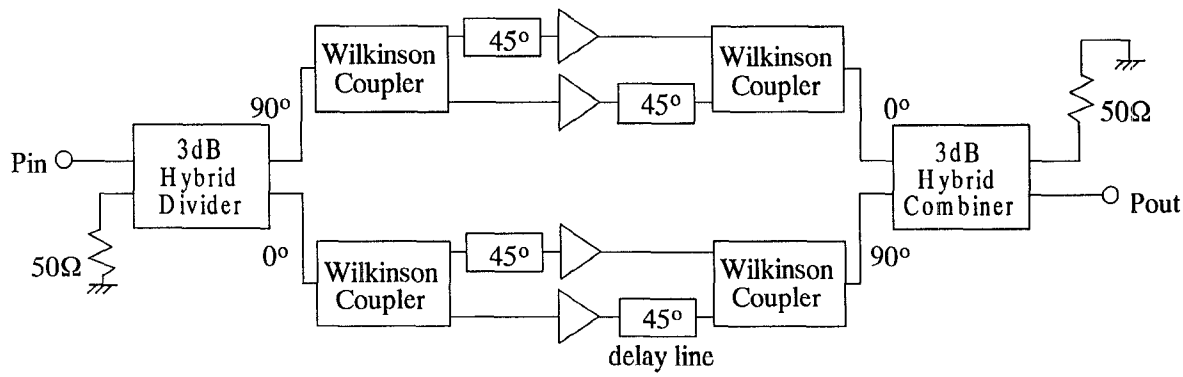

Fig. 4 Configuration of the experimental four-paralleled amplifier.

VSWR=2,3,5. The distortion under -45dBc, the efficiency over 45% and the gain over 9.8dB were obtained for load VSWR ≤ 3. The amplifier had the distortion of -53dBc, the efficiency of 51% and the gain of 11.1dB with 50Ω load, considering each 0.3dB loss of both the divider and the combiner. The variations of the distortion, efficiency and gain for a fixed load VSWR are accounted for by the small performance variations among the four elemental amplifiers.

5. Conclusion

We proposed a new four-paralleled power amplifier combined in different phases in order to accomplish a low distortion and high efficiency in wide range of load impedances. We studied them from the characteristics of a elemental amplifier unit by simulation and experiment for four-paralleled amplifier. The adjacent channel leakage power for π/4-DQPSK modulation was improved 13dB in comparison with a conventional amplifier in range of load VSWR ≤ 3 without decreasing efficiency.

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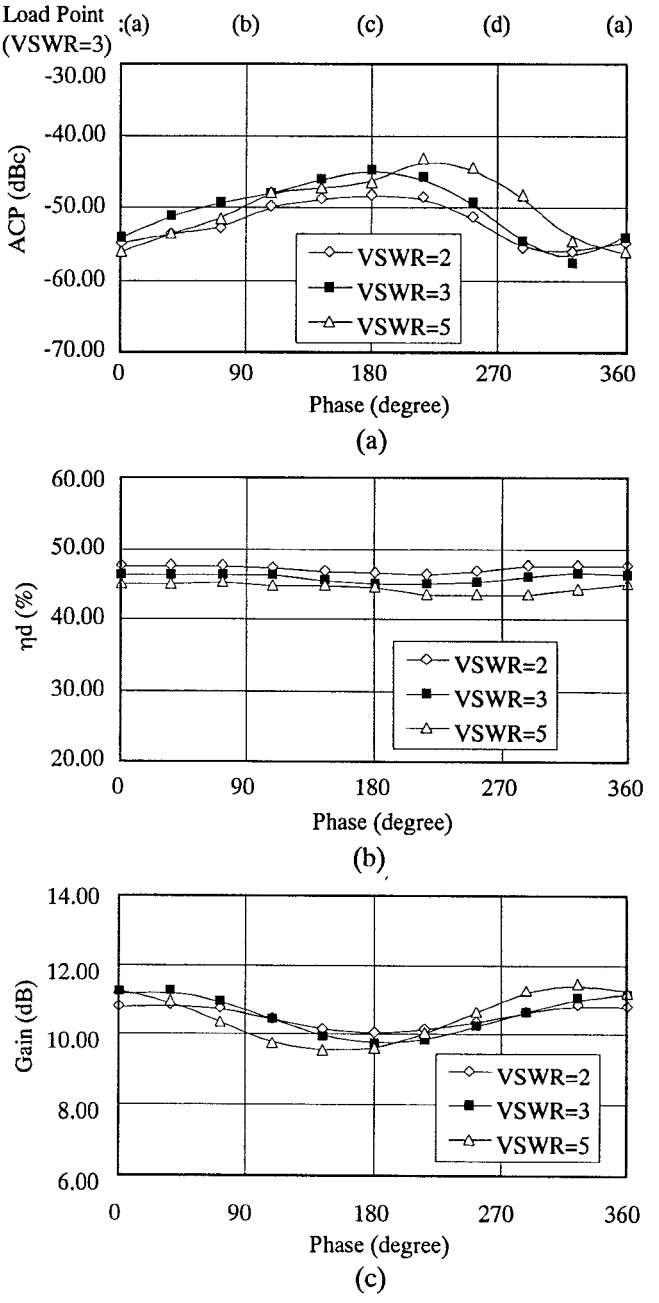

Fig. 5 Characteristics of the experimental four-paralleled amplifier with respect to load impedance.
Pout=35dBm, Vd=3.5V, Freq.=948MHz
(a) Adjacent channel leakage power (ACP)
(b) Drain efficiency
(c) Gain